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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* ISAO OKADA, TSUYOSHI HIRABUKI, and NORIYUKI  
KOTANI

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Appeal 2009-003667  
Application 10/693,928  
Technology Center 2600

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Decided: August 26, 2009

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Before KENNETH W. HAIRSTON, KARL D. EASTHOM, and ELENI  
MANTIS MERCADER *Administrative Patent Judges.*

EASTHOM, *Administrative Patent Judge.*

DECISION ON APPEAL

## STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 1-16, all the pending claims (Br. 4).<sup>1</sup> Subsequent to the appeal, the Examiner withdrew the rejections to claims 2, 6, 7, 9, 10, 13, 14, and 16 (Ans. 2). Therefore, the rejections of claims 1, 3-5, 8, 11, 12, and 15 are before us. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants invented, according to their disclosure, a recording pulse generator (for writing data onto a disc) which performs plural signal processing in one delay line. The delay line has plural circuit delay elements 2b each of which generates a different clock phase shift. A level shift stage 22 comprising multiple level shifters shifts the levels of the clocks and generates "fine" clocks T0-T15. A recording pulse width is controlled based on a selected clock. (Abstract; Fig. 1; Spec. 8:17-25; 12:23-25).

Exemplary claim 1 follows:

1. A recording pulse generator comprising:  
a first delay line having plural circuit elements cascaded in multiple stages, wherein the first delay line outputs plural output clocks each having different phase differences with a clock inputted to the first stage of the first delay line, according to the number of stages of the plural circuit elements thereof;

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<sup>1</sup> Appellants' Brief (filed Oct. 29, 2007) ("Br.") and the Examiner's Answer (mailed Feb. 7, 2008) ("Ans.") detail the respective positions of the parties and are referenced herein.

a level shift stage that shifts the levels of the plural output clocks to generate plural fine clocks, respectively;  
a selector that selects an arbitrary fine clock from the plural fine clocks generated;  
and a recording pulse generator that generates a recording pulse on the basis of a fine clock selected.

The Examiner relies on the following prior art references:

Kobayashi	US 5,818,805	Oct. 6, 1998
Iijima	US 2002/0051415 A1	May 2, 2002
Hayashi	US 6,493,305 B1	Dec. 10, 2002
Okada	US 2004/0090889 A1	May 13, 2004

The Examiner also relies on certain portions of Appellants' disclosure as Appellants' admitted prior art (*hereinafter* "AAPA"), including Figure 13 and its accompanying description in the Specification (*see infra* FF 1).

The Examiner rejected under 35 U.S.C. § 103(a), claims 1 and 4 based upon Iijima and the AAPA; claims 3 and 8 based on Iijima, the AAPA, and Hayashi; claims 5 and 12 based on Iijima, the AAPA, and Kobayashi; and claims 11 and 15 based on Iijima, the AAPA, Hayashi, and Kobayashi.

### ISSUE

Appellants contest (Br. 8) the Examiner's finding that Appellants' description of Figure 13 as "conventional art" constitutes an admission that the conventional art is admitted as prior art. Appellants also contest (Br. 13) the Examiner's finding that the Iijima and the AAPA collectively teach a delay line comprising fine clocks and a level shift stage as set forth in claim 1. Thus, the following issue is before us: Did Appellants demonstrate that the Examiner erred in finding that Iijima and the AAPA collectively teach or suggest fine clocks and a level shift stage as set forth in claim 1?

## FINDINGS OF FACT (FF)

### *Appellants' Disclosure*

1. According to Appellants, the conventional recording pulse generator includes a delay line 11 having a series of cascaded inverters 2b creating selectable clocks at 16 taps 11a. The clock signals are tapped and delayed at 11a by every two stages of inverters 2b and thereafter selected by a selection means 21, and then shifted by a level shifter 22 and input to an OR circuit 22 to create recording pulses. (Spec. 5:1-5; 6:22-29; Fig. 13). Appellants also refer to the conventional art as prior art; i.e., “any disclosed document of the prior art was not found” (Spec. 8:5-6).

### *Iijima*

2. Figure 1 of Iijima depicts a pulse recording circuit comprising a delay line 11, which

receives the first clock signal SCK1 and outputs the respective outputs of the delay elements 11a as a delay clock signal group SCK2. In other words, the delay clock signal group SCK2 is a set of signals each having a difference phase difference from the first clock signal SCK1.

(¶0033).

3. “A selector 12 selects one delay clock signal from the delay clock signal group SCK2 output from the delay line 11, and outputs the selected delay clock signal as a prescribed delay clock signal SCK2i” (¶0034).

Selector 12 receives a control signal S1 to select a specific delay clock signal SCK2i (*id.*, Fig. 1).

## PRINCIPLES OF LAW

“[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a prima facie case of unpatentability.” *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). “On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.” *In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)). To establish a prima facie case, “‘there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness,’” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *Kahn*, 441 F.3d at 988).

## ANALYSIS

Appellants assert a legal distinction between admitted “prior art” and “conventional art” (Br. 8-11). However, inasmuch as Appellants’ argument (Br. 13) that “[e]ven if the AAPA is included in the rejection, . . . the level shift stage 22 in Fig. 13 of the present application does not teach or suggest that the level shift stage may be used to generate fine clocks to be selected by the selector” is persuasive of error, whether or not the asserted legal distinction exists, need not be decided. (*See also* Br. 13 (concluding “the absence of the claimed source of fine clocks”)).

The Examiner relied on the combined teachings of figure 1 of Iijima (teaching plural delayed clocks (FF 2, 3))<sup>2</sup> and figure 13 of the AAPA (teaching a level shift stage 22, (FF 1)) to teach the corresponding plural fine clocks as set forth in claim 1 (Ans. 4-5, 10-14). The clocks become “fine” according to claim 1 after the level shift stage, and are, according to the Examiner, “fine” based on the combination of the AAPA level shift stage 22 and Iijima’s delay line clocks 11a (*see* FF 2, Ans. 4-5, 10-14).

The Examiner also articulated several reasons (i.e., “to provide proper signal level for circuit operation” and “rearranging parts . . . involves only routine skill in the art” (Ans. 14)) why skilled artisans would have placed the AAPA level shift stage 22 prior to Iijima’s selector 12 (Ans. 14) to arrive at the claimed plural fine clocks (*see also* Ans. 4-5, 13-14). *See KSR*, 550 US at 417 (a mere arrangement of parts is likely obvious).

However, the AAPA only discloses one level shifter 22. The Examiner does not articulate how plural fine clocks emanate from one level shifter so that “a selector . . . selects an arbitrary fine clock from the plural fine clocks generated” as required by claim 1. Nor is it clear how, according to the Examiner’s response, merely placing the selector after a level shifter 22 creates plural fine clocks. The Examiner also does not set forth any finding that plural level shifters would have been obvious. While it is conceivable that claim 1 does not necessarily require such plural level shifters, the Examiner does not articulate how one level shifter creates plural fine clocks.

The Examiner summarizes:

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<sup>2</sup> The Examiner additionally found that the AAPA also discloses plural clocks (Ans. 13-14).

The claimed invention utilizes a delay line to generate plural output clocks, utilizes the level shift stage to generate plural fine clocks, selects a fine clock from the plural fine clocks and utilizes the selected fine clock to generate a recording pulse while AAPA discloses a delay line to generate plural output clocks, selecting a clock from the plural clocks, utilizing a level shift stage to generate a fine clock from the selected clock and generating a recording pulse from the fine clock. Whether the level shifting occurs before or after the clock selection is inconsequential because ultimately, both the claimed invention and the combination of the prior art disclose generating a recording pulse from a fine clock which is derived from plural output clocks.

(Ans. 14).

The Examiner's summary and other findings noted *supra* fall short of an articulated reasoning as to how the combination creates plural fine clocks. To establish a prima facie case, "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness," *KSR*, 550 U.S. at 418 (quoting *Kahn*, 441 F.3d at 988).

Therefore, Appellants have demonstrated error in the Examiner's rejection of claim 1 and dependent claim 4. With respect to claims 3 and 8, 5 and 12, and 11 and 15, the added teachings of Hayashi, Kobayahsi, and Hayashi and Kobayahsi, respectively fail to cure the noted shortcomings in the teachings of Iijima and AAPA. Accordingly, Appellants also have demonstrated error in the Examiner's rejection of these claims.

In view of the above discussion, we will not sustain the Examiner's 35 U.S.C. § 103 rejections of claims 1, 3-5, 8, 11, 12, and 15.



### CONCLUSION

Appellants demonstrated that the Examiner erred in finding that Iijima and the AAPA collectively teach or suggest plural fine clocks as set forth in claim 1.

### DECISION

We reverse the Examiner's decision rejecting claims 1, 3-5, 8, 11, 12, and 15.

REVERSED

gvw

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